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(54) LVDS receiver using differential amplifiers

(57) An interface arrangement including the cascade connection of a differential pre-amplifier (HPA1, HPA2) and a comparator (DA), and generally known as fast Low Voltage Differential Signal [LVDS] circuit for interfacing electronic chips. The current standards for such a LVDS circuit specify a minimum switching threshold voltage for the small differential input signal, while the common mode input signal varies over a very large range, both at a very high frequency. This is achieved owing to the fact that the differential pre-amplifier comprises a first (HPA1) and a second (HPA2) half pre-amplifier, each receiving the arrangement inputs (INN, INP) in an opposite way. Each half pre-amplifier (HPA1/HPA2) having first input inverter means (NN1, PN1) coupling an input (INN/INP) to an output (OUT1/OUT2) thereof, and second input inverter means (NP1, PM1, PM2; PP1, NM1, NM2) coupling the other input (INP/INN) to the output via current mirror means (PM1, PM2; NM1, NM2). The output current of the second input inverter means is thereby inverted with respect to the output current of the first input inverter means. To obtain a controlled gain, the half pre-amplifier further includes a short-circuited inverter.

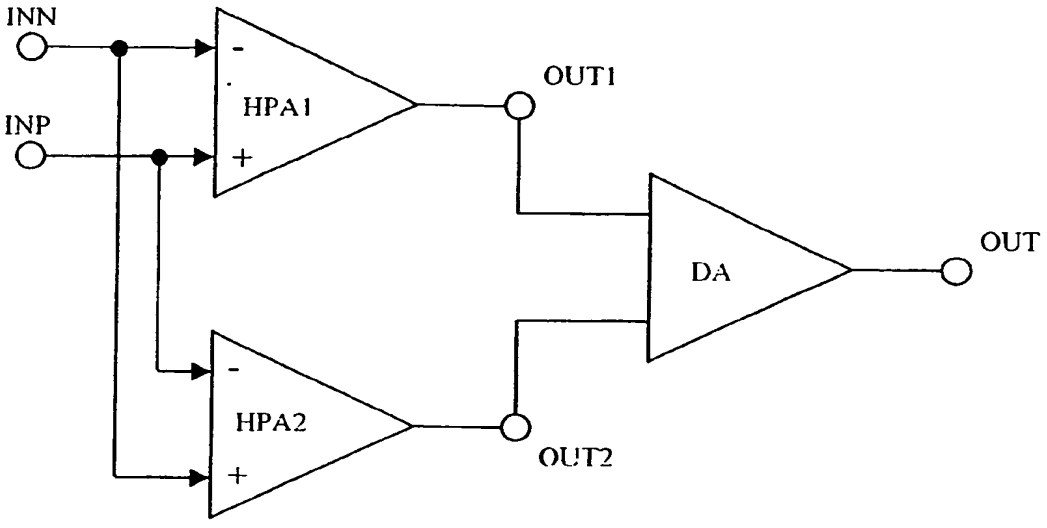

Fig. 1

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Description

[0001] The present invention relates to an interface arrangement including a very high speed pre-amplifier for operating with relatively small input signals and with high Common Mode Rejection [CMR]. More particularly, the invention relates to an interface arrangement including, between a differential pair of inputs and an output, the cascade connection of a differential pre-amplifier and a comparator.

[0002] Such an interface arrangement is generally known in the art as a fast Low Voltage Differential Signal [LVDS] circuit for interfacing electronic chips. The current standards for such a LVDS circuit specify a minimum switching threshold voltage for the small differential input signal, while the common mode input signal varies over a very large range, both at a very high frequency. Because of the small input signal, a high sensitivity is required from the interface arrangement. In the known interface arrangements, the comparator is a differential amplifier preceded by a very high-speed differential pre-amplifier with low and controlled gain. The pre-amplifier must amplify the differential signal and attenuate the common mode signal. A simple differential pair of either NMOS transistors or PMOS transistors is not able to work in this full input range. Therefore, two input differential pairs are generally put in parallel: a PMOS and a NMOS differential pair. The outputs of these two differential pairs are combined into the inputs of the comparator. Each differential pair spans a part of the input voltage range. In the middle of this voltage range both PMOS and NMOS input pairs are active, whilst for input voltages near to the ground or to the supply voltage, either only the PMOS inputs or only the NMOS inputs are active. As a consequence, the gain of the input pre-amplifier is not constant over the whole input voltage range. Traditional circuits to keep the gain constant are much too slow for complying the standard requirements and can thus not be used. Moreover, since the output of the known pre-amplifier is related to the ground or to the supply voltage, the design of the subsequent comparator or differential amplifier is more difficult. Also the offset changes between each region of operation and this has a direct impact on the signal skew.

[0003] An object of the present invention is to provide an interface arrangement of the above known type but wherein the gain is constant over the relatively large input voltage range for a relatively small input signal.

[0004] According to the invention, this object is achieved due to the fact that said differential pre-amplifier comprises a first and a second half pre-amplifier, each of said half pre-amplifiers having a first and a second input and an output connected to a distinct input of said comparator, that the first input of said first half pre-amplifier is connected to a first input of said interface arrangement and is coupled to the output of said first half pre-amplifier via first input inverter means, whilst the second input of said first half pre-amplifier is connected to the second input of said interface arrangement and is coupled to said output via second input inverter means comprising current mirror means for inverting the output current of said second input inverter means with respect to the output current of said first input inverter means, that said second half pre-amplifier is similar to said first half pre-amplifier, and that the first input of said second half pre-amplifier is connected to the second input of said interface arrangement, whilst the second input of said second half pre-amplifier is connected to the first input of said interface arrangement.

[0005] In this way, opposite currents coming from the first and from the second input inverter means are provided to the output of each half pre-amplifier. Since the two half pre-amplifiers are oppositely connected with respect to each other, a very high common mode signal attenuation is obtained. The inverter means behaves as an amplifier with the full supply voltage as input range. As a result, the large common mode range can be covered. A very high-speed is also possible owing to the low skew between the signals and the signal input range can be as wide as the full supply voltage.

[0006] Another characteristic feature of the present invention is that said first input inverter means comprises a first NMOS transistor series connected with a first PMOS transistor between a first supply terminal and a second supply terminal, the first input of said interface arrangement being connected to the gate of each of said first NMOS and first PMOS transistors, and the junction point of said series connected transistors being connected to the output of said half pre-amplifier.

[0007] The present invention is further also characterized in that said second input inverter means comprises a first and a second inverting circuit, in that said first inverting circuit comprises a second NMOS transistor series connected with a mirror input PMOS transistor between the first and the second supply terminals, in that said second inverting circuit comprises a second PMOS transistor series connected with a mirror input NMOS transistor between said first and said second supply terminals, in that the second input of said interface arrangement is connected to the gate of each of said second NMOS and second PMOS transistors, in that said second input inverter means further comprises a mirror output NMOS transistor series connected with a mirror output PMOS transistor between said first and said second supply terminals, the gate and the drain of said mirror input PMOS transistor being connected to the gate of said mirror output PMOS transistor, and the gate and the drain of said mirror input NMOS transistor being connected to the gate of said mirror output NMOS transistor, and in that the junction point of said series connected mirror output transistors being connected to the output of said half pre-amplifier.

[0008] As the NMOS and PMOS transistors behave quadratically, the sum of their gains remains constant. As a result, the gain of the interface arrangement re-

mains constant over the full range of the input voltage.

[0009] Also another characteristic feature of the present invention is that a current source is provided between the gate of said mirror input PMOS transistor and the gate of said mirror input NMOS transistor.

[0010] This current source, located between the two diode connected mirror input transistors, prevents these transistors from switching both off when one of them is switched off at the extremes of signal input range. In other words, the current source keeps the two current mirrors active. As a result of which the speed of the Common Mode Rejection [CMR] is high.

[0011] Yet another characteristic feature of the present invention is that each of said half pre-amplifier further includes output means comprising an output NMOS transistor series connected with an output PMOS transistor between the first and the second supply terminal, the gates of said output NMOS and PMOS transistors being connected to the output of said half pre-amplifier as well as their junction point.

[0012] The complementary transistors are so forming a short-circuited inverter. This circuit is equivalent to a voltage source in series with a resistor. The resistance thereof is inversely proportional to the transconductance gain of the inverter transistors. In this way, a controlled gain can be achieved. Moreover, the dc voltage at the half pre-amplifier output is then around the mid supply voltage. This is usually better for the comparator and for the skew performance of a subsequent circuit, that may for instance be a pulse shaper.

[0013] Further characteristic features of the present interface arrangement are mentioned in the appended claims.

[0014] The above and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

Fig. 1 represents a fast interface arrangement according to the invention;
Fig. 2 shows a NMOS branch of a half pre-amplifier (HPA1) forming part of the fast interface arrangement of Fig. 1; and
Fig. 3 shows the half pre-amplifier (HPA1) including the branch of Fig. 2.

[0015] The fast interface arrangement of the invention is a Low Voltage Differential Signal [LVDS] circuit used for interfacing electronic chips. The arrangement therefore needs to be conform to the current LVDS standards IEEE - 1596.3 (1996) and TIA / EIA - 644 (1996), which specify a minimum switching threshold voltage of 100 mVolt for the differential input signal, while the Common Mode input signal varies from 0.0 to 2.40 Volt, for a 3.3 Volt supply voltage. Additionally, the signal speed for the current applications is 250 MHz and the Common Mode signal speed is specified up to 1 GHz.

[0016] To achieve these requirements. the interface arrangement comprises a fast pre-amplifier followed by a comparator. The pre-amplifier is adapted to amplify (≅ +10 dB) the differential input signal and to attenuate (for at least -20 dB) the common mode signal before the comparator.

[0017] As shown at Fig. 1, the interface arrangement has differential input terminals INN and INP and output terminal OUT. The pre-amplifier is constituted by two half pre-amplifiers HPA1 and HPA2 and is connected to a comparator DA constituted by a differential amplifier. In more detail, the input terminal INN is connected to the inverting input (-) of the half pre-amplifier HPA1 and to the non-inverting input (+) of the half pre-amplifier HPA2, whilst the input terminal INP is symmetrically connected to the non-inverting input (+) of HPA1 and to the inverting input (-) of HPA2. Output OUT1 of HPA1 is connected to an input of the comparator DA and output OUT2 of HPA2 is connected to the other input DA, the output of DA being connected to the output terminal OUT.

[0018] Each half-pre-amplifier HPA1/HPA2 is made of two parallel branches of opposite polarity: a NMOS branch and a PMOS branch. The NMOS branch of the half pre-amplifier HPA1 is for instance shown at Fig. 2. In this branch, the input terminal INN is connected to the gate of a NMOS input transistor NN1 whose source is connected to the ground Vss and whose drain is connected to the output OUT 1. The input terminal INP is connected to the gate of another NMOS input transistor NP1 whose source is also connected to the ground Vss but whose drain is connected to the output OUT1 via a PMOS current mirror circuit. The current mirror circuit inverts the drain current of NP1 and is constituted by two PMOS transistors PM1 and PM2 having their gates interconnected and connected to the drain of PM1. The drain of NP1 is connected to the drain of PM1 whose source is connected to the supply terminal Vdd. The source of PM2 is also connected to Vdd and its drain is connected to the output OUT1.

[0019] Whilst the drain current of the first NMOS input transistor NN1 is directly applied to the output OUT1, the current generated by the second NMOS input transistor NP1 is inverted via the PMOS current mirror circuit PM1, PM2 and fed back into the drain of the first NMOS input transistor NN1. If the input signals INN and INP, at the two like-named input terminals, are at the same voltage, both NMOS currents cancel each other and there is no output signal at OUT1, irrespective of their common mode voltage. On the contrary, if the two input signals INN and INP differ by a differential voltage, the NMOS currents do not cancel and there is an output current available at OUT1.

[0020] A complementary circuit is built with PMOS transistors to form, together with the NMOS branch of Fig. 2, a full half pre-amplifier, say HPA1, as shown at Fig. 3. This complementary circuit comprises the PMOS transistors PN1 and PP1 and a NMOS current mirror

circuit with NMOS transistors NM1 and NM2. The input terminals INN and INP are connected to the gates of the PMOS transistors PN1 and PP1 respectively. PN1 is connected between the supply terminal Vdd and the drain of NN1, i.e. the output terminal OUT1, whilst PP1 is connected to the supply terminal Vdd and to the output terminal OUT1 via the NMOS current mirror circuit NM1, NM2. These transistors NM1 and NM2 have their gates interconnected and connected to the drain of NM1 and their sources connected to the ground Vss. The drain of NM1 is connected to the drain of PP1, whilst the drain of NM2 is connected to the output terminal OUT1.

[0021] The series connection of the transistors NN1 and PN1 between the ground Vss and supply terminal Vdd constitutes a first input inverter for the half pre-amplifier HPA1, whilst the input transistors NP1, PP1 together with the current mirrors PM1, PM2 and NM1, NM2 constitute a second input inverter for HPA1. An input inverter is an amplifier with the full supply as input range. As a result, the large common mode range can be covered.

[0022] The input terminal INN can be seen as being connected to the inverting input (-) of the first half pre-amplifier HPA1, whilst the input terminal INP can be seen as being connected to the non-inverting input (+) of HPA1.

[0023] The output current of the combined NMOS branch and PMOS branch is converted into an output voltage OUT1 at the like-named output terminal. This is performed by means of a short-circuited inverter as will be described below.

[0024] The short-circuited inverter comprises NMOS transistor NO1 and PMOS transistor PO1 as shown at the Figs. 2 and 3. These transistors are series connected between the ground Vss and supply terminal Vdd, with their junction point connected to the output terminal OUT1. The gates of NO1 and PO1 are also together connected to the output terminal OUT1. A short-circuited inverter is equivalent to a voltage source in series with a resistor. The resistance is inversely proportional to the transconductance gain of the inverter transistors. As a result, a controlled gain can be achieved.

[0025] Finally, a current source I1 is added between the two diode connected transistors PM1 and NM1 of the current mirrors. This current source I1 prevents these transistors both from switching off when one of the input PMOS or NMOS transistors, PM1 or NM1, is switched off at the extremes of signal input range. In other words, the current source I1 keeps the current mirrors active and thereby keeps the speed of the Common Mode Rejection [CMR] high.

[0026] It is to be noted that the W/L of the transistors NO1 and PO1 forming the short-circuited inverter is smaller than that of the NMOS and PMOS input transistors NN1, NP1, PN1 and PP1 mentioned above. The ratio of these W/Ls controls the differential gain of the half pre-amplifier HPA1.

[0027] To form the whole pre-amplifier of the interface arrangement, the second half pre-amplifier HPA2 is added to HPA1 with both input terminals INN and INP exchanged. The half pre-amplifier HPA2 is identical to HPA1. As a result, HPA2 has the same common mode output voltage value and the inverse differential output voltage as HPA1. In more detail, and referring again to Fig. 1, the input terminal INN of the interface arrangement is connected to the inverting input (-) of the first half pre-amplifier HPA1 and to the non-inverting input (+) of the second half pre-amplifier HPA2, whilst the input terminal INP of the arrangement is connected to the non-inverting input (+) of HPA1 and to inverting input (-) of HPA2. As already mentioned, the two complementary outputs OUT1 and OUT2 of respectively HPA1 and HPA2 are fed to the differential comparator DA.

[0028] Since the PMOS and NMOS transistors of the pre-amplifiers behave quadratically, the sum of their gains remains constant. The gain of the interface arrangement thus remains constant over the full input range. The present interface arrangement also works for low supply voltages, as long as the supply voltage Vdd remains larger than $Vt_N + Vt_P + 2*(Vgs - Vt)$, where Vt is the threshold voltage, Vt_N and Vt_P respectively for the NMOS and the PMOS transistors, and Vgs is the gate-to-source voltage of these transistors.

[0029] While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention, as defined in the appended claims.

Claims

1. Interface arrangement including, between a differential pair of inputs (INN; INP) and an interface output (OUT), the cascade connection of a differential pre-amplifier (HPA1, HPA2) and a comparator (DA), characterized

   in that said differential pre-amplifier comprises a first (HPA1) and a second (HPA2) half pre-amplifier, each of said half pre-amplifiers having a first (-) and a second (+) input and an output (OUT1; OUT2) connected to a distinct input of said comparator (DA),
   in that the first input (-) of said first half pre-amplifier (HPA1) is connected to a first input (INN) of said interface arrangement and is coupled to the output (OUT1) of said first half pre-amplifier via first input inverter means (NN1; PN1), whilst the second input (+) of said first half pre-amplifier (HPA1) is connected to the second input (INP) of said interface arrangement and is coupled to said output (OUT1) via second input inverter means (NP1, PM1, PM2; PP1, NM1, NM2) comprising current mirror means (PM1,

PM2; NM1, NM2) for inverting the output current of said second input inverter means with respect to the output current of said first input inverter means,
in that said second half pre-amplifier (HPA2) is similar to said first half pre-amplifier (HPA1), and
in that the first input (-) of said second half pre-amplifier (HPA2) is connected to the second input (INP) of said interface arrangement, whilst the second input (+) of said second half pre-amplifier (HPA2) is connected to the first input (INN) of said interface arrangement.

2. Interface arrangement according to claim 1, characterized in that said first input inverter means (NN1; PN1) comprises a first NMOS transistor (NN1) series connected with a first PMOS transistor (PN1) between a first supply terminal (Vss) and a second supply terminal (Vdd), the first input (INN) of said interface arrangement being connected to the gate of each of said first NMOS (NN1) and first PMOS (PN1) transistors, and the junction point of said series connected transistors (NN1, PN1) being connected to the output (OUT1; OUT2) of said half pre-amplifier.

3. Interface arrangement according to claim 1, characterized in that said second input inverter means (NP1, PM1, PM2; PP1, NM1, NM2) comprises a first and a second inverting circuit,

in that said first inverting circuit comprises a second NMOS transistor (NP1) series connected with a mirror input PMOS transistor (PM1) between a first supply terminal (Vss) and a second supply terminal (Vdd),
in that said second inverting circuit comprises a second PMOS transistor (PP1) series connected with a mirror input NMOS transistor (NM1) between said first (Vss) and said second (Vdd) supply terminals,
in that the second input (INP) of said interface arrangement is connected to the gate of each of said second NMOS (NP1) and second PMOS (PP1) transistors,
in that said second input inverter means further comprises a mirror output NMOS transistor (NM2) series connected with a mirror output PMOS transistor (PM2) between said first (Vss) and said second (Vdd) supply terminals, the gate and the drain of said mirror input PMOS transistor (PM1) being connected to the gate of said mirror output PMOS transistor (PM2), and the gate and the drain of said mirror input NMOS transistor (NM1) being connected to the gate of said mirror output NMOS transistor (NM2), and
in that the junction point of said series connected mirror output transistors (NM2, PM2) being connected to the output (OUT1; OUT2) of said half pre-amplifier.

4. Interface arrangement according to claim 3, characterized in that a current source (I1) is provided between the gate of said mirror input PMOS transistor (PM1) and the gate of said mirror input NMOS transistor (NM1).

5. Interface arrangement according to claim 1, characterized in that each of said half pre-amplifier further includes output means comprising an output NMOS transistor (NO1) series connected with an output PMOS transistor (PO1) between a first supply terminal (Vss) and a second supply terminal (Vdd), the gates of said output NMOS and PMOS transistors being connected to the output (OUT1; OUT2) of said half pre-amplifier as well as their junction point.

6. Interface arrangement according to claim 1, characterized in that, in each half pre-amplifier (HPA1; HPA2), said first input is an inverting input (-) and said second input is a non-inverting input (+).

7. Interface arrangement according to claim 6, characterized in that said comparator (DA) is a differential amplifier, and
in that the output (OUT1) of said first half pre-amplifier is connected to a first input of said comparator, whilst the output (OUT2) of said second half pre-amplifier is connected to a second input of said comparator.

8. Interface arrangement according to any of the claims 2, 3 or 4, characterized in that said first supply terminal (Vss) is at the ground and in that said second supply terminal (Vdd) is at the supply voltage.

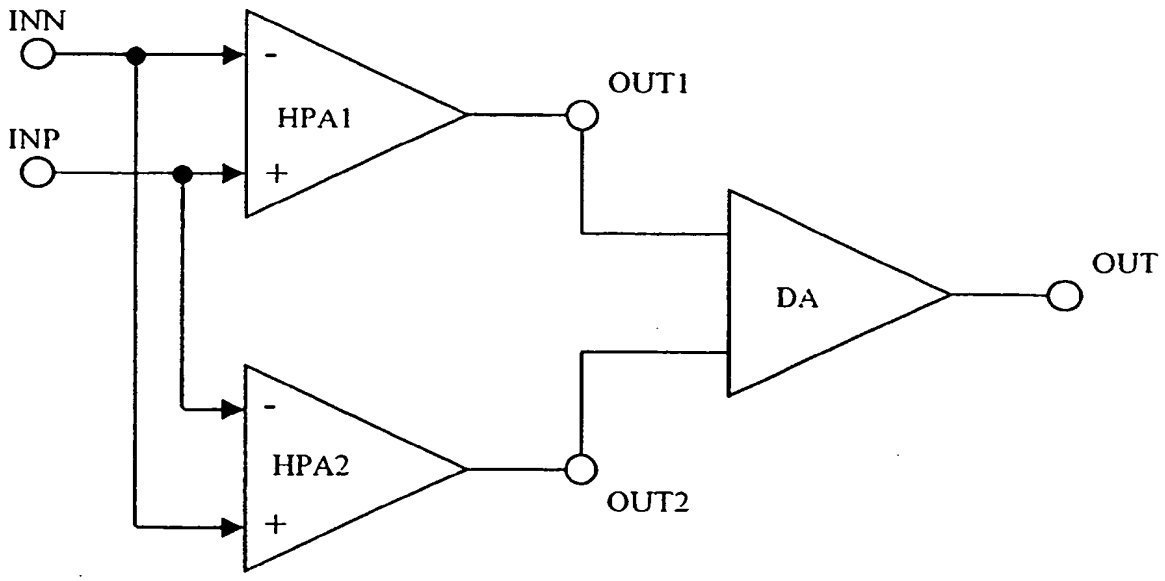


Fig. 1

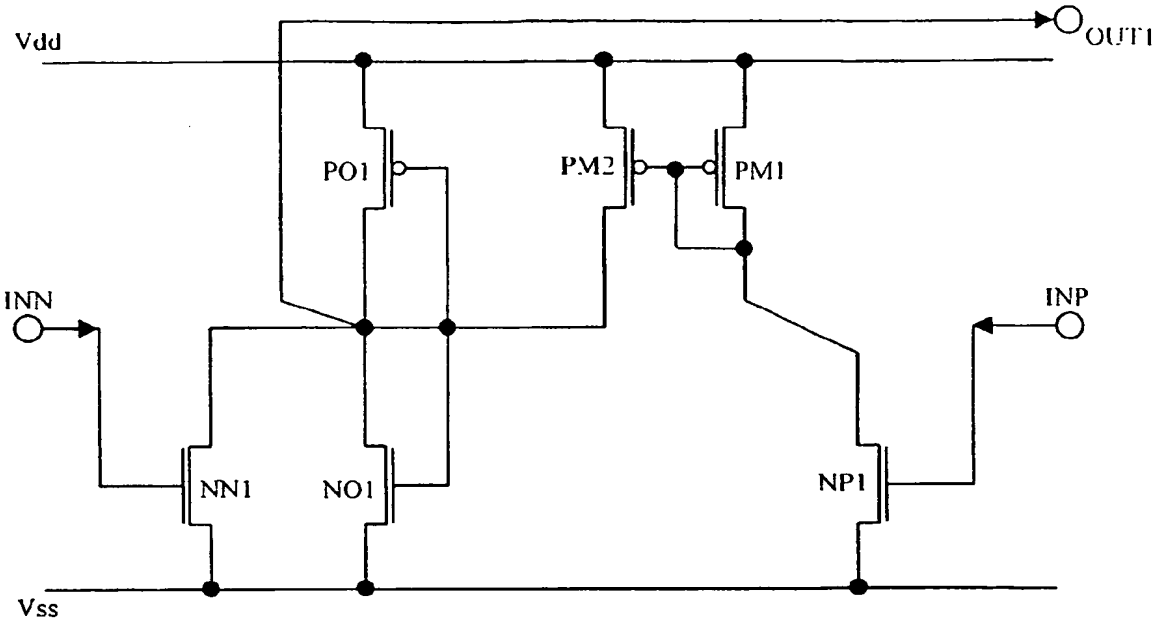
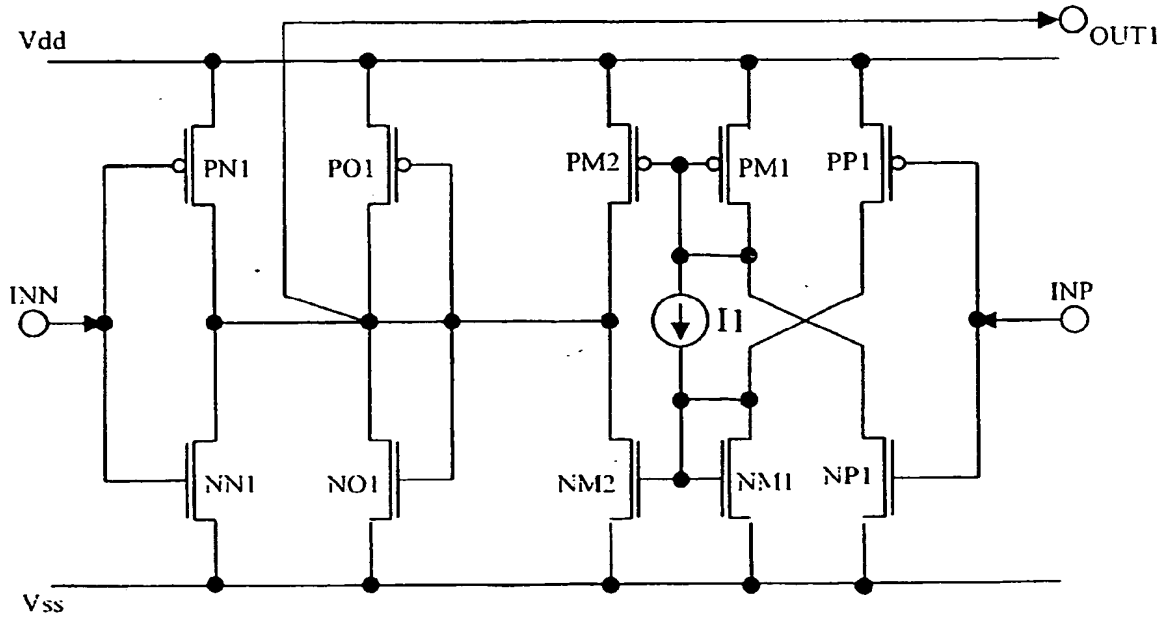


Fig. 2



HPA1

Fig. 3

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EUROPEAN SEARCH REPORT

Application Number
EP 99 40 1622

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03K
H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 November 1999	Butler, N

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